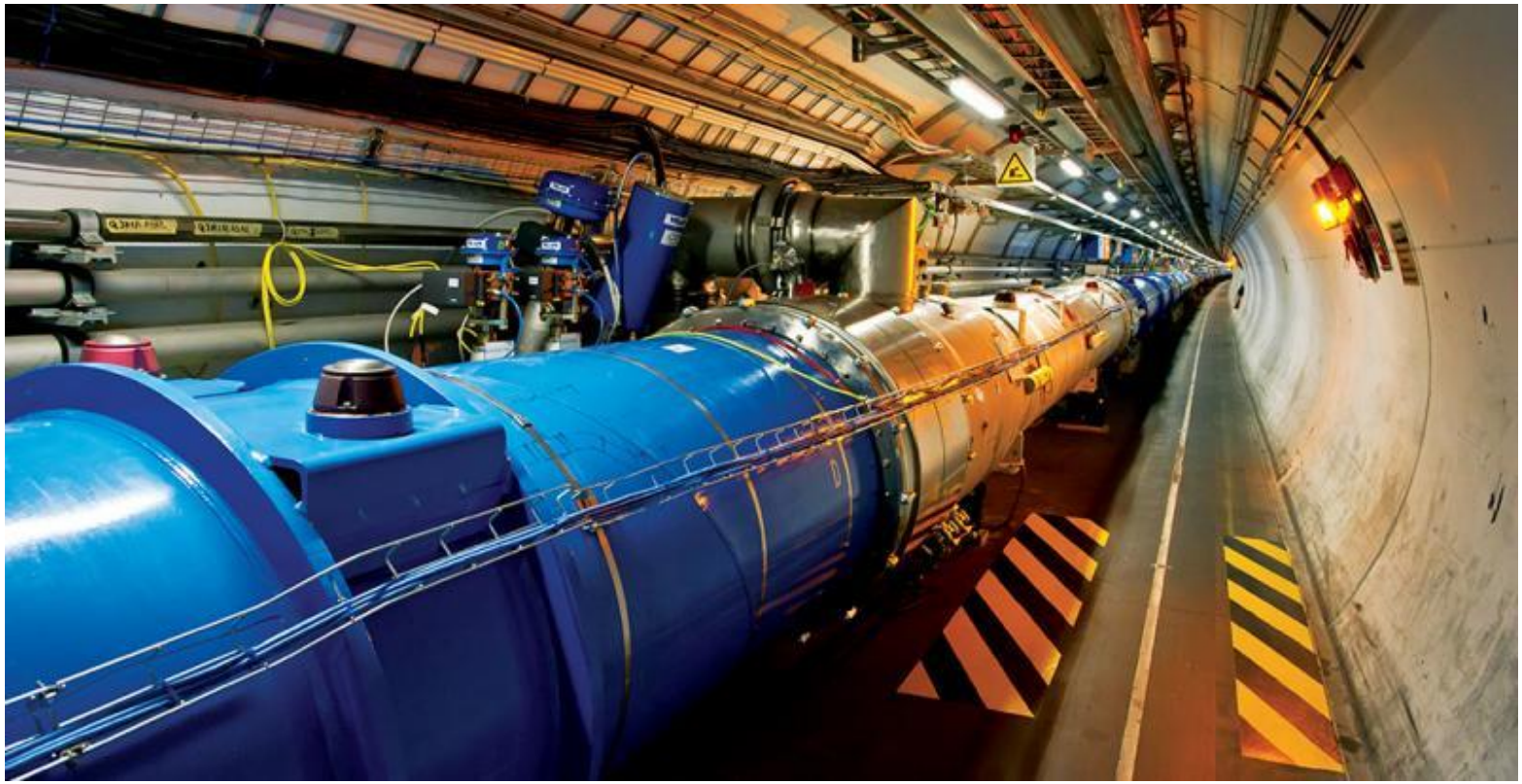


High DR ADC for LHC

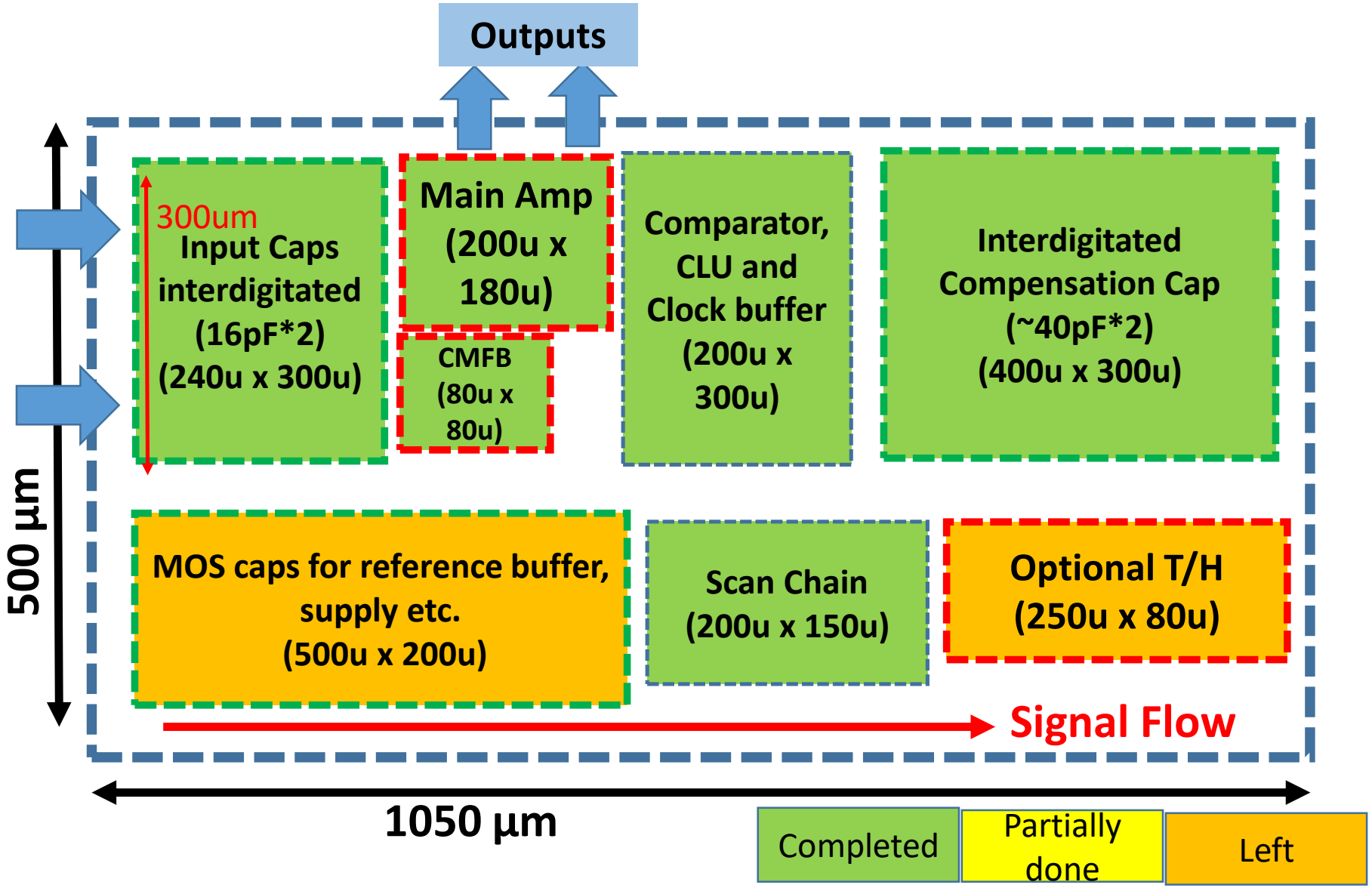
Sarthak Kalani

Last updated: 04/28/17

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

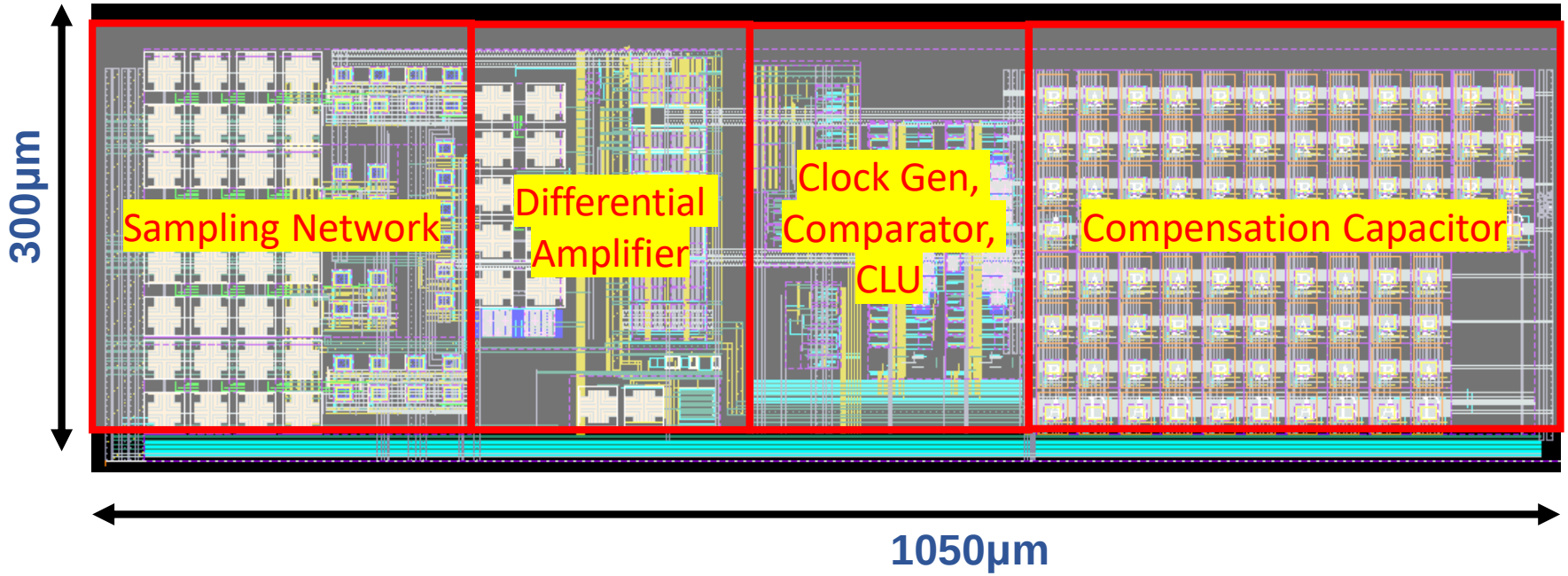
Columbia Integrated Systems Laboratory

DRE block layout scheme



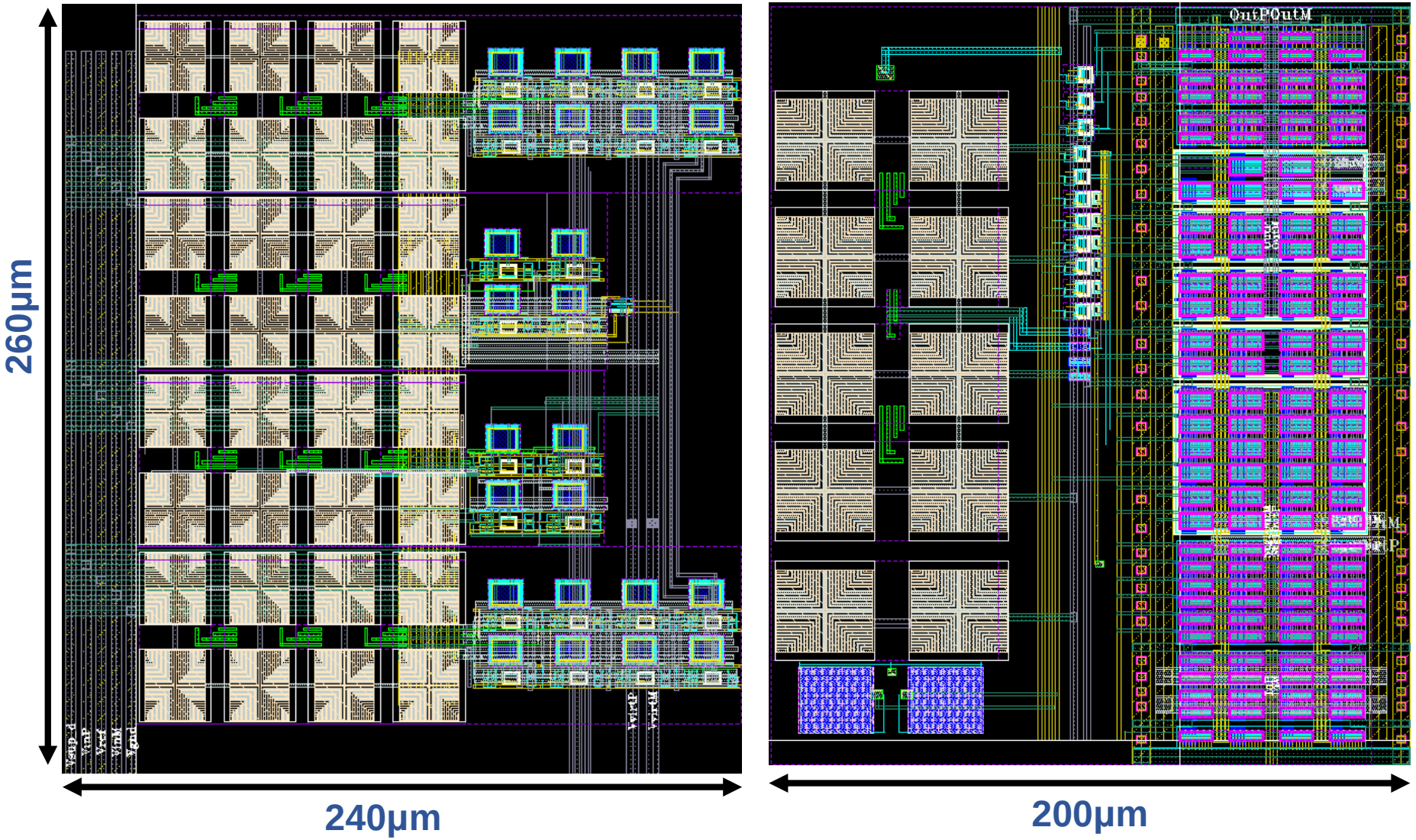
Channel area: 950 µm x 300 µm, Active area: 950 µm x 500 µm

Layout Status update

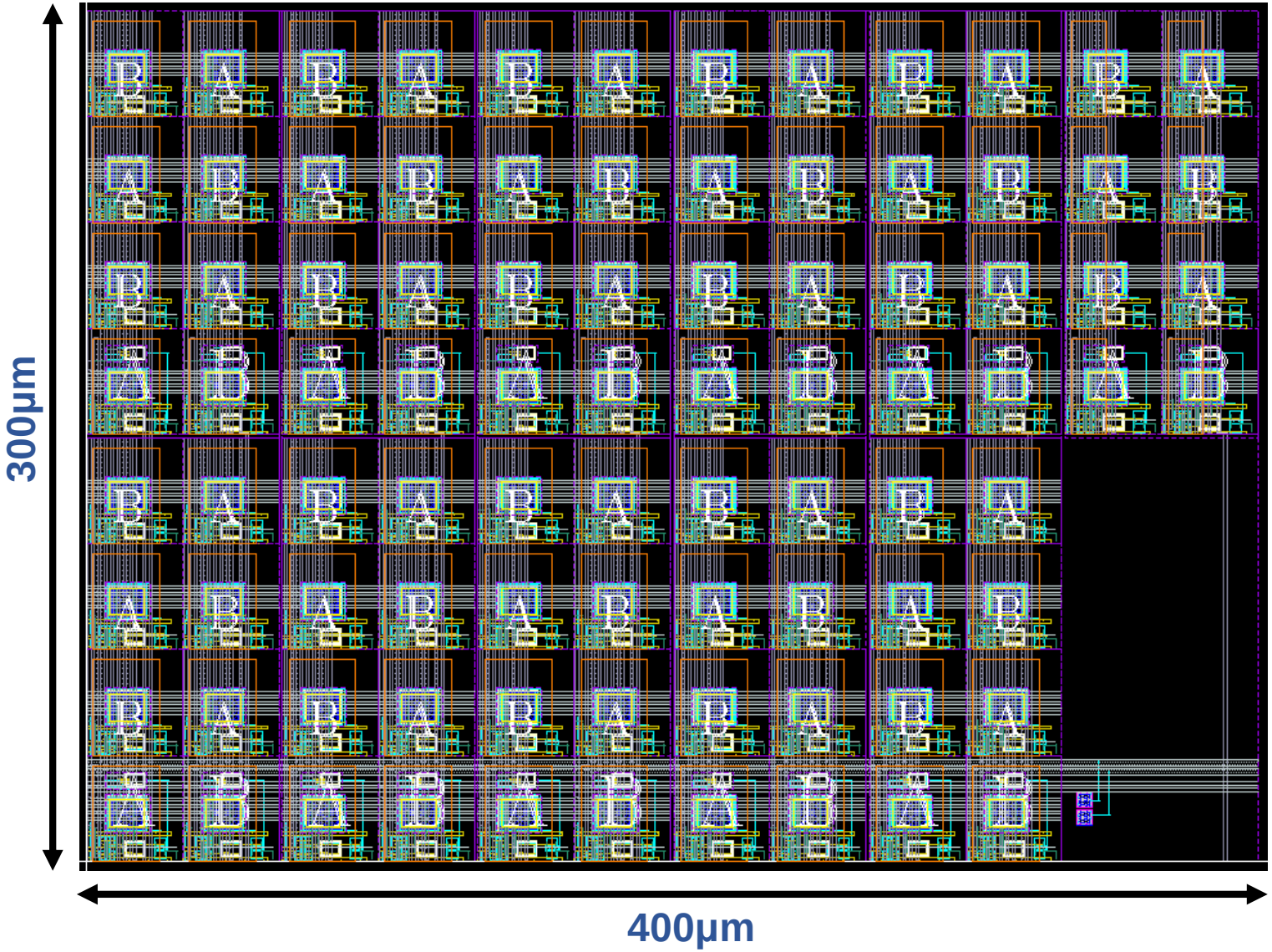


- Completed all the individual blocks
- On the last stage of integration
- Should be done with top routing by this weeknend.

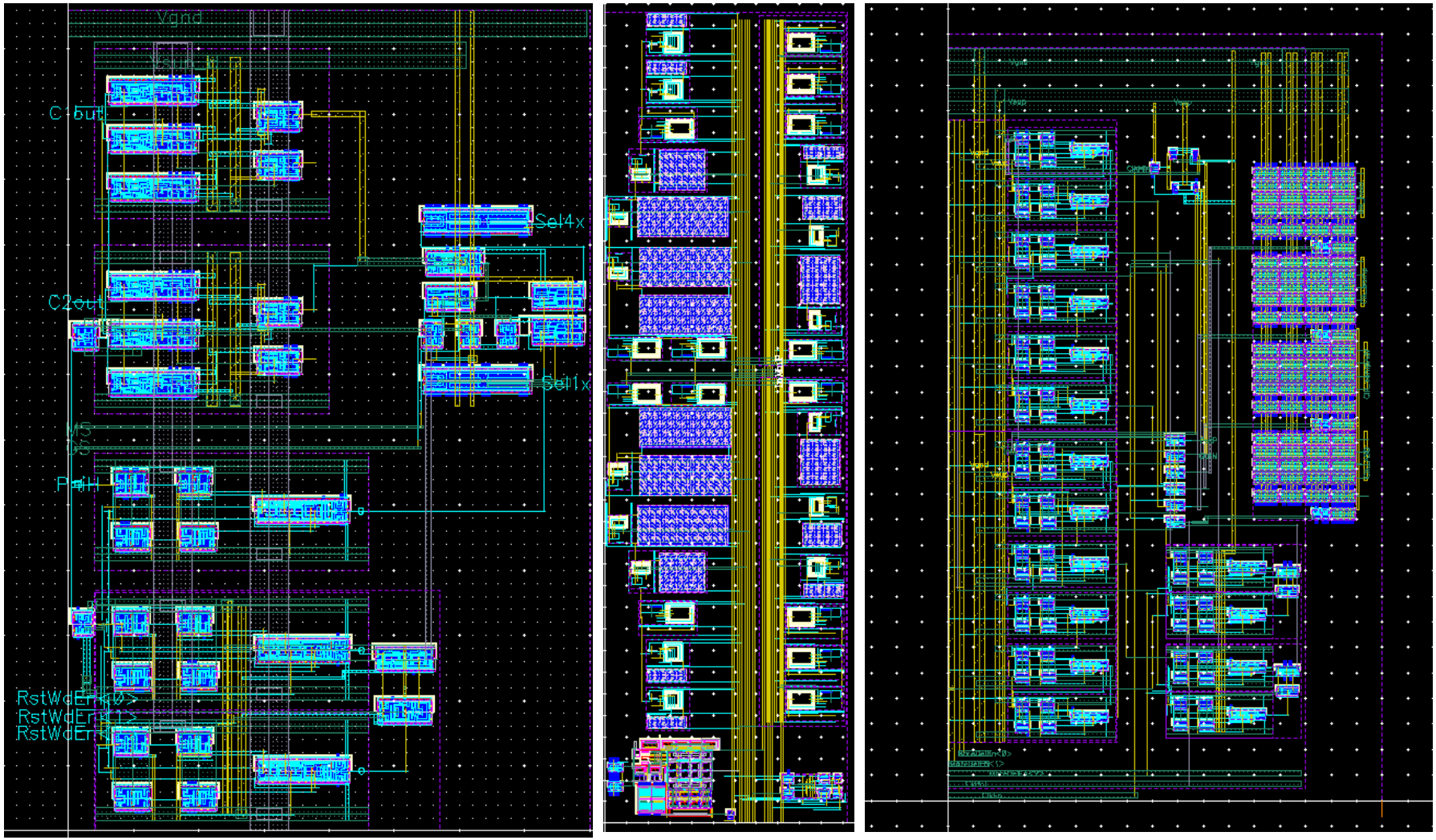
Sampling network and Differential Amplifier



Miller Compensation Capacitor



Clock Generator, Comparator & CLU



Verification Steps

S.No.	Topic	Priority	Time required	To be tested by				Comments
				Jaro	Chen-Kai	Ray	Sarthak	
System level testing								
1	Complete schematic at top level, create a testbench	1	By April 28th	x	x	x	x	Work in progress. 2 meetings happening a week for updates. Tentatively complete by April 28th
2	**Test clock timings**							
a	Clock to SAR, DRE, Scan Chain, Serializer in top level schematic, tt27.	1	0.5 days	x	x	x		Check driving capability and margins
b	Check DRE output (it should settle) and compare with the clock used for sampling by SAR block. Schematic level, tt 27	1	1 day		x	x	x	Check for timing margin
c	Check serializer clock in detail, synchronize with SAR outputs. Schematic, works on corner cases in schematic level	1	1 day	x	x	x	x	SK to make sure Decision bit stays valid at the end of load cycle.
			20					
3	Scan chain testing: Ability to drive bits. Check across corners, introducing intentional bit error and correction. Readout operation	1	1 day	x				
4	Driver and receiver: correct operation, with proper load? Across PVT?	1	0.5 days	x				
5	2 a, b, c testing in schematic, PVT	2	1 day	x	x	x	x	

- Verification sheet created to track progress for next 3 weeks.

Next steps

- Complete DRE block layout
- Start simulations on top level
- Start top level integration to produce first gds by May 7th